LISTING OF CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

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1. (Currently Amended) A system comprising:

a component;

a detector to detect a power management event; and

a controller to transition, in response to the power management event, a first setting of the component from a first performance mode to a second performance mode,

the controller to transition the component ~~to~~ from a reduced activity state, a core component clock remains active during the reduced activity state, and the controller to change a second setting of the component from a first performance mode to a second performance mode.

2. (Original) The system of claim 1, wherein the component is the processor.

3. (Original) The system of claim 1, wherein changing the first setting of the component includes changing the core processor supply voltage level from a first voltage level to a second, higher voltage level.

4. (Original) The system of claim 1, wherein the reduced activity state includes the sleep state.

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5. (Original) The system of claim 1, wherein changing the second setting of the component includes changing the core processor clock frequency from a first frequency level to a second, higher frequency level.

6. (Currently Amended) The system of claim ~~4~~ 1, wherein the core processor clock remains active during the sleep state.

7. (Currently Amended) The system of claim ~~4~~ 1, wherein a system clock input to the processor remains active during the sleep state.

8. (Original) The system of claim 1, wherein the power management event includes a change of the system power source from an internal power source to an external power source.

9. (Original) The system of claim 1, wherein changing the first setting of the component can requires 500 microseconds.

10. (Original) The system of claim 1, wherein changing the second setting of the component requires less than 5 microseconds.

11. (Currently Amended) A system comprising:

a component;

a detector to detect a power management event;

a controller to transition the component, in response to the power management event, to a reduced activity state, a core component clock remains active during the reduced activity state,

the controller to change a first setting of the component from a first performance mode to a second performance mode,

the controller to transition ~~the component out of the reduced activity state, and to transition~~ a second setting of the component from a first performance mode to a second performance mode.

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12. (Original) The system of claim 11, wherein the component is the processor.

13. (Original) The system of claim 11, wherein the reduced activity state includes the sleep state.

14. (Original) The system of claim 11, wherein changing the first setting of the component includes changing the core processor clock frequency from a first frequency to a second, lower frequency.

15. (Original) The system of claim 11, wherein changing the second setting of the component includes changing the core processor supply voltage level from a first voltage level to a second, lower voltage level.

16. (Currently Amended) The system of claims 13~~1~~, wherein a system clock input to the processor remains active during the sleep state.

17. (Currently Amended) The system of claims 13~~1~~, wherein the core processor clock remains active during the sleep state.

18. (Original) The system of claim 11, wherein the power management event includes a change of the system power source from an external power source to an internal power source.

19. (Original) The system of claim 12, wherein changing the first setting of the component requires less than 5 microseconds.

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20. (Original) The system of claim 11, wherein changing the second setting of the component can requires 500 microseconds.

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21. (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, the set of instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event;

transitioning a first setting of a component from a first performance mode to a second performance mode in response to the power management event,

transitioning the component ~~to~~ out of a reduced activity state, a core component clock remains active during the reduced activity state, and to change a second setting of the component from a first performance mode to a second performance mode,

if the power management event includes the system power source switching from an internal power source to an external power source; and

transitioning the controller to ~~a~~ the reduced activity state in response to the power management event,

changing the second setting of the component from the second performance mode to the first performance mode,

transitioning the component ~~out of~~ to the reduced activity state, and transitioning the ~~second~~ first setting of the component from the second performance mode to the first performance mode,

if the power management event includes the system power source switching from an external power source to an internal power source.

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22. (Original) The computer-readable medium of claim 21, wherein the first setting of the component includes the core processor supply voltage level.

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23. (Original) The-computer readable medium of claim 21, wherein the component is the processor.

24. (Original) The computer-readable medium of claim 22, wherein the second performance mode includes a higher voltage level than the first performance mode.

25. (Currently Amended) The computer-readable medium of claim 21, wherein the reduced activity state includes a ~~the~~ sleep state.

26. (Currently Amended) The computer-readable medium of claim 25~~1~~, wherein the core processor clock remains active during the sleep state.

27. (Original) The computer-readable medium of claim 21, wherein the second setting of the component includes the core processor clock speed.

28. (Original) The computer-readable medium of claim 27, wherein the second performance mode includes a higher frequency level than the first performance mode.

29. (Currently Amended) The computer-readable medium of claim 25~~1~~, wherein a system clock input to the processor remains active during the sleep state.

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30. (Canceled) ~~The computer-readable medium of claim 21, wherein changing the second setting of the component requires 500 microseconds.~~

31. (Currently Amended) An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller to transition, in response to the indication, transition a power supply voltage level of a component from a first level to a second, higher level, the controller to transition the component ~~to~~ from a low activity state, a core component clock remains active during the low activity state, and to change a core component clock frequency from a first level to a second, higher level, while the component is in the low activity state.

32. (Original) The apparatus of claim 31, wherein core component clock and a system clock input to the component remain active during the low activity state.

33. (Original) The apparatus of claim 31, wherein the indication is generated in response to a change in a power source in the system from an internal power source to an external power source.

34. (Currently Amended) An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller to transition the component to a low activity state in response to the indication, a core component clock remains active during the low activity state,

the controller to change the component core clock frequency from a first level to a second, lower level, ~~while the component is in the low activity state, the controller to transition the component out of the reduced activity state,~~ and to transition a power supply voltage level of the component from a first level to a second, lower level.

35. (Original) The apparatus of claim 34, wherein the core component clock and a system clock input to the component remain active during the low activity state.

36. (Original) The apparatus of claim 34, wherein the indication is generated in response to a change in a power source in the system from an external power source to an internal power source.